GaAs MONOLITHIC LUMPED ELEMENT MULTISTAGE MICROWAVE AMPLIFIER

K.P. Weller, G.D. Robinson
A. Benavides, R.D. Fairman

TRW Electronic Systems Group
Redondo Beach, California

ABSTRACT

This paper reports on the successful development of a four stage, directly cascaded GaAs FET monolithic preamplifier chip realized using truly lumped elements for both RF and DC circuitry. The chip is designed to be entirely self-biased and contains all required DC circuitry on-chip for operation from a single drain supply. The design is based on a nominal 1 micron gate length interdigital FET geometry of planar construction. The device is fabricated using a selective ion implantation process. The finished die dimensions are 0.060 by 0.110 inch with a thickness of 0.015 inch. The chip provides a gain of over 20 dB in a 2 GHz band centered near 7 GHz. The noise figure achieved is 6 dB, the output power at 1 dB gain compression is typically +8 dBm, and the third order intermodulation intercept point is approximately +20 dBm.

INTRODUCTION

As a building block circuit for more complex GaAs MMIC receiver chip development, there is a need for a general purpose family of wideband amplifier configurations which consume a minimal chip area and provide significant gain with moderate noise and power performance. Considerations which must enter into the design of circuits to satisfy this requirement include physical size, simplicity in biasing, yield, and performance uniformity, as well as the RF performance specifications. The GaAs MMIC amplifier reported in this paper was designed to satisfy this requirement for an X-band receiver.

The amplifier chip developed provides over 20 dB gain with a 6 dB noise figure in the 6 to 8 GHz frequency range. The circuit configuration is completely monolithic and uses lumped elements, exclusively, for both RF matching and DC biasing. This minimizes the chip area consumed by the passive circuit elements. The design is a four stage directly cascaded amplifier which includes self-biasing. All DC circuitry is contained on the chip for operation from a single drain supply voltage. An interdigital FET geometry with a nominal 1 micron gate length is used in each stage. A planar selective ion implantation process is used to realize the FET profile with good isolation between devices in the IC. The FET design and fabrication process does not yield state-of-art device performance but was chosen to provide good yield and uniformity in processing. In the following sections of this paper, the design, fabrication, and RF characterization of the GaAs MMIC amplifier are discussed in more detail.

AMPLIFIER SCHEMATIC DESIGN AND MONOLITHIC LAYOUT

In developing an electrical design for a microwave amplifier to be realized in monolithic form, a number of compromises must be made. If the design is to compete in performance with its hybrid MIC equivalent, the FET design and process technology must be entirely equivalent to that of the hybrid discrete device. Also, the matching network loss incurred in the MMIC must be similar to that of the hybrid. In X-band, this generally means that distributed element matching must be used in the monolithic circuit. If a primary objective is to achieve low noise performance, the input match must be designed to provide optimum noise loading to the FET input. This will result in a relatively poor impedance match at the input to the amplifier. Recent work by Lehmann and coworkers has shown that an MMIC designed in this manner can yield very good RF performance.[1] However, the distributed matching elements consume a relatively large amount of GaAs real estate. Also, the uniformity resulting from current materials and processing techniques employed to achieve state-of-art FET device characteristics is questionable.

In most applications, the impedance match at the input and output of an amplifier must be reasonably good. A single-ended, noise-matched FET input stage will generally not provide the required match. In hybrid circuits, this problem is overcome by using a balanced design which incorporates a coupler to provide isolation between the stage input and the mismatch at the FET input. The coupler is relatively large, making it an undesireable addition to an MMIC design. An alternative approach which seems natural for a monolithic realization is to use active matching on the chip which, in principle, can result in a good match with minimal noise figure degradation. Preliminary results have been reported on the use of a common gate input stage in an MMIC multistage amplifier chip.[2] This approach should yield a near optimum match over a broad band with small sacrifice in the noise

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measure of the first stage.

Schematic Design

The present amplifier design does not address the matching problem associated with noise performance optimization. Instead, both input and output matching networks were designed with the objective of achieving a good impedance match. A common source configuration is used in each stage. Acceptable noise figure is obtained, for many applications, simply by biasing the FET in the first stage to a current level where noise performance is generally good. The matching networks for the amplifier were based on an empirically derived data base on the FET used. The data base was developed through extensive characterization of discrete devices, biased at both low noise and high gain bias. To establish a set of S-parameters which could be used for monolithic design, the effect of the bond wire inductance associated with the discrete device was removed from the measured data.

The network topology for input, output, and interstage matching was developed based on equivalent input and output circuit models for the FET derived from the measured S-parameter data base. The device models used were derived using the negative image method[3] with the aid of an optimization routine in the COMPACT computer-aided design program. In this method, input and output matching networks consisting of negative value reactive elements and lossless ideal transformers are optimized over the frequency band of interest. The element values in these ideal networks are optimized to achieve the best possible conjugate matched simultaneously at input and output. The optimized element values are used to derive the input and output models for the device. The input and output models derived are thus based on all four S-parameters.

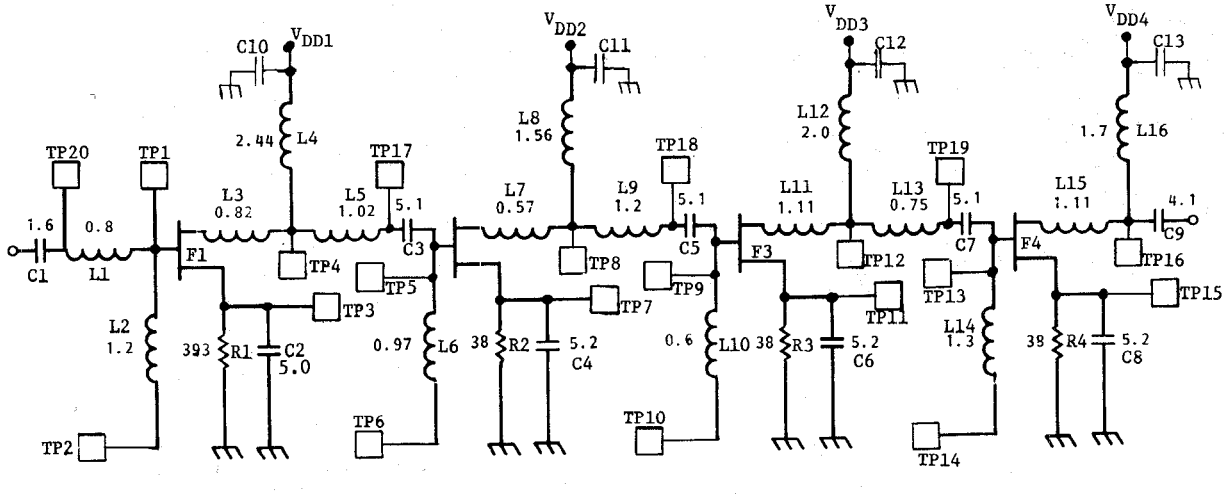
The gain calculated for the FET with optimized negative image networks at input and output is the maximum available gain from the stage and can be used to determine the minimum number of stages required to achieve the desired gain. It was determined in this manner that a minimum of four stages is required to achieve more than 20 dB gain with the intended FET. The calculated maximum available gain as a function of frequency also indicates the amount of gain compensation required in the interstage matching networks to produce a flat gain response over the frequency range of interest. The FET with conjugate matching at input and output has an inherent gain rolloff between 5 and 6 dB per octave for both low noise and high gain bias.

The development and optimization of the matching and interstage networks proceeded as follows:

1) Lossless, realizable network topologies were synthesized and optimized for conjugately matching to the input of the FET at low noise bias and the output at high gain bias.

2) Interstage matching networks were developed which provide the appropriate gain compensation to achieve a flat response in the four stage amplifier. Each interstage network provides approximately 8 dB per octave in positive gain slope as a function of frequency.

3) The entire amplifier circuit was then analyzed and reoptimized with the introduction of appropriate loss elements which result from the finite Q of the network elements.



RESISTORS IN OHMS
CAPACITORS IN pF
INDUCTORS IN nH

Figure 1: Schematic Diagram of Four Stage, Single-Ended GaAs FET MMIC Chip

The final schematic diagram of the four stage amplifier circuit is shown in Figure 1. In addition to the optimized reactive matching network elements, source resistors with bypass capacitors are included in the design so that the amplifier can be self-biased. The resistor values chosen were based on the measured bias conditions on the FETs used for generating the initial design data base. The first stage bias resistor was chosen to be consistent with the low noise bias condition. The remaining stages were biased for high gain. The schematic also indicates a number of test pads in the circuit. These were designed into the layout to simplify the DC screening of the amplifier chips.

Chip Layout

The layout of the amplifier circuit (see chip photograph in Figure 2) was performed with the aid of the computer system APPLICON. The layout is designed to provide maximum flexibility in both DC screening and RF evaluation of the chips. A large number of test pads are provided to allow the DC probing of most of the active and passive components in the circuit individually. Although the design is intended for self-biased operation, the DC grounding of the gates is not made on the chip. Also, a bonding pad is provided which will permit overriding the self-biasing resistor in each stage. Through the bonding configuration selected, each stage can be either self-biased or biased with independent gate voltage control. To achieve fully self-biased operation, each gate pad must be DC grounded and all drain pads must be bonded together and connected to a single drain bias supply. In the RF evaluation which has been performed to date, the self-biasing has been used for the last three stages in the amplifier and the first stage is independently biased.

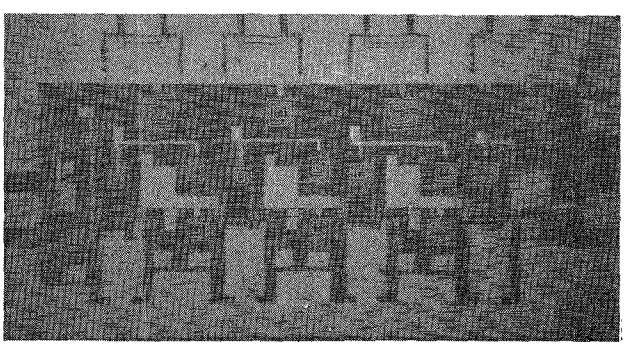


Figure 2: Photograph of GaAs MMIC Amplifier Chip

GaAs MMIC AMPLIFIER FABRICATION PROCESS

A relatively simple seven mask level process was used for the fabrication of the MMIC amplifier chips. The process employs selective ion implantation of silicon into qualified GaAs semi-insulating substrate material for the formation of active channel and ohmic contact regions in the FETs and bulk resistors used for self-biasing. In order to easily obtain good alignment to the selective implants, a special alignment mark is defined on the wafer to which all implant and subsequent metal deposition mask levels are aligned. The process begins with the sputter deposition of a thin layer of Si_3N_4 onto the cleaned surface of the GaAs substrate. This layer protects the surface and provides some surface stabilization during processing. All ion implants are performed through the thin Si_3N_4 layer. The alignment mark is deposited on top of this layer. Using thick photoresist for masking, the channel and ohmic contact region implants are then completed. Prior to performing the high temperature anneal, a sputter deposited layer of SiO_2 is added on top of the Si_3N_4 as an additional cap. The anneal is performed in a furnace at 850°C for 20 minutes.

Following implant anneal, the ohmic contact and Schottky gate metal depositions are performed. A conventional liftoff technique is used to define the ohmic metal pattern. A thin GeAu alloy is e-beam deposited and subsequently alloyed to form the ohmic contacts to the N^+ implanted regions on the GaAs. The gate metal pattern is used to define all interconnection patterns on the lower level as well as all Schottky gates. In order to deposit a thick gate metal pattern with good resolution, a special double resist liftoff technique is used to define the gate metal. The Schottky gate metallization used is TiPtAu which is deposited normal to the surface in an e-beam evaporator. This technique results in a gate length near 1 micron and a gate thickness of greater than 1 micron.

The passive elements and interconnections in the MMIC are formed using a two level system separated by a plasma deposited Si_3N_4 layer. All lower level interconnections, bottom plates of capacitors, etc., are defined in the gate metal pattern as mentioned previously. Following deposition of the gate metal, a thick layer of Si_3N_4 is deposited over the entire surface of the wafer. Via holes are then etched in the dielectric where contact must be made to the lower level metal pattern. Finally, the top metal pattern is defined using the double resist liftoff technique. In this case the technique is designed to allow for the deposition of approximately 3 microns of metal in order to minimize the RF loss in passive elements. The metal system used is TiAu deposited in an e-beam system. The top metal pattern is used to define most interconnections, inductor spirals, and top plates of capacitors.

MMIC AMPLIFIER CHIP CHARACTERIZATION

The amplifier chips were mounted in a simple microstrip test fixture for characterization. After some preliminary evaluation it was determined that the self-bias resistor value chosen for the first stage is too high for optimum overall amplifier performance. Therefore, the chips were bonded using the self-biasing only for the last three stages. The drain pads for the last three stages were tied together using wire bonding and connected to a single power supply. The first stage was bi-

ased independently to achieve the best noise measure in the first stage. Therefore a total of three supply voltages were required in testing the chips.

The RF evaluation performed on the amplifier chip includes gain-frequency response, noise figure as a function of frequency, dynamic behavior at selected frequencies, and third order intermodulation distortion at midband. In performing a complete set of measurements, the same bias conditions were used for all measurements on a particular chip, and absolutely no external tuning was used. The RF performance reported includes all loss or mismatch due to the test fixture. No attempt was made to subtract fixture loss. For the RF data presented in Figures 3 through 5, the following bias conditions were used on a selected chip typical of the better devices from the first wafer processed:

First Stage Gate Voltage-	-3.5 V
First Stage Drain Voltage-	3.0 V
First Stage Drain Current-	11.5 mA
Remaining Stages Drain Voltage-	3.7 V
Remaining Stages Drain Current-	211.0 mA

The gain and noise figure performance of the amplifier chips were characterized on an automatic network analyzer, and both sweeped and point-by-point noise figure measurement systems, respectively. The results for the selected chip are shown in Figure 3. The peak gain achieved is slightly under 23 dB at 6.5 GHz, and the noise figure approaches 6 dB at a slightly higher frequency. The output power as a function of input power, with frequency as a parameter, is shown in Figure 4. The power output for 1 dB gain compression near midband is +8 dBm. The third order intermodulation distortion was measured using an equal amplitude two tone input signal with 100 MHz separation. A plot of the total fundamental output power and total intermodulation output as a function of total input power is shown in Figure 5. By straight line extrapolation, the third order intermodulation intercept (IP_3) is determined to be +20 dBm. It should be noted that the anomalies sometimes reported for FET amplifiers with regard to intermodulation distortion measurements were not observed in measurements on this chip. The intermodulation distortion curves are well behaved to power levels exceeding the 1 dB compression point and therefore the intercept has value as a figure of merit for the amplifier.

Although the RF results reported here are preliminary, they are typical of several chips measured from the first wafer processed. The best chip, in terms of bandwidth, had slightly over 20 dB peak gain and a 3 dB bandwidth of 6.3 to 8.4 GHz. The minimum noise figure for this chip was also 6 dB and the IP_3 is +16 dBm at midband.

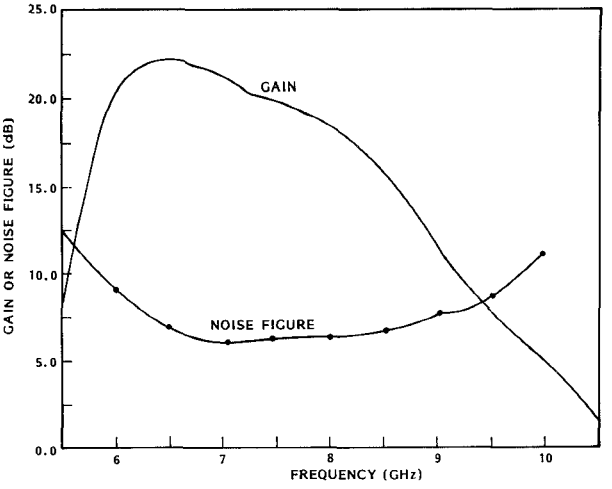


Figure 3: Gain and Noise Performance as a Function of Frequency for MMIC Amplifier

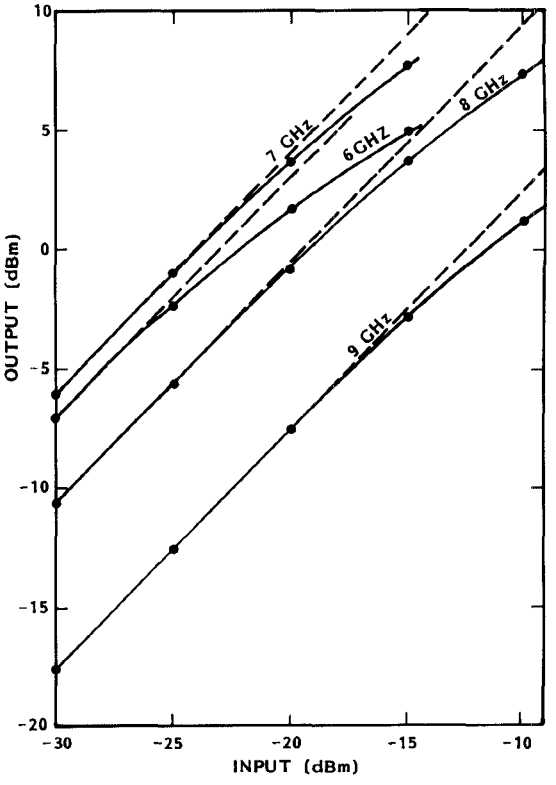


Figure 4: Dynamic Characteristics of MMIC Amplifier

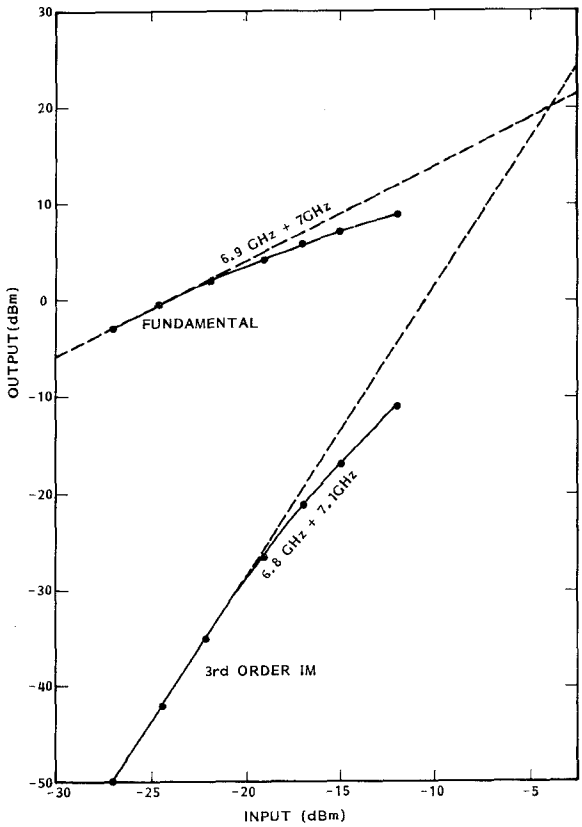


Figure 5: Third Order Intermodulation Characteristics of MMIC Amplifier

CONCLUSION

The preliminary results obtained on the first wafer processed for the MMIC amplifier design discussed here are very encouraging. Some improvement in performance is anticipated with further processing, but significant improvement will come with a design iteration. Although the self-biasing concept has been shown viable, improved control over the resistor value would be beneficial. Evaluation of discrete devices fabricated along with the amplifier chip indicates that the resistor value for the last three stages could be increased significantly to reduce the drain current without significant gain reduction. This would not only reduce DC power consumption but also improve noise figure. Once a complete analysis of this first iteration design is complete, the necessary iterations in design will be implemented.

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ACKNOWLEDGEMENT

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